Gayatri Vidya Parishad College of Engineering for Women
(Autonomous)
B.Tech - I Semester Regular Examinations Dec/Jan - 2025
Elements of Electronics Engineering - 24EC11RC04
Solutions

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1 a Mass action law:

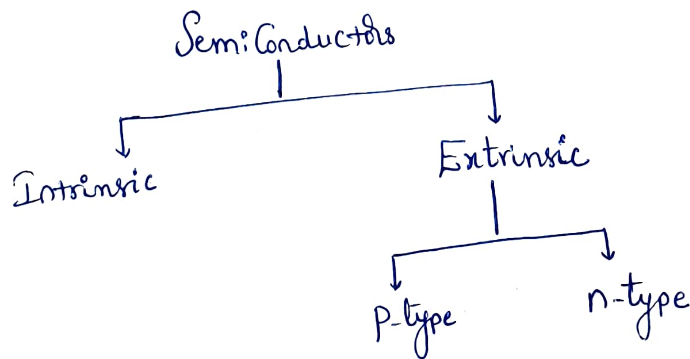
It states that the product of number of electrons in the Conduction band (n) and the number of holes in the Valance band (P) is Constant at a fixed temperature. The law is applicable irrespective of amount of doping.

Mathematically the law is Expressed as

$$np = n_i^2$$

where $n_i \rightarrow$ Intrinsic Carrier Concentration

Types of SemiConductors:



Intrinsic SemiConductor:
A pure SemiConductor is Called intrinsic SemiConductor which has Equal no. of electrons and holes.

Extrinsic SemiConductor:
Doped SemiConductor material is Called Extrinsic SemiConductor. Adding impurities to a pure Semi Conductor is Called doping. The impurity modifies the electrical properties of the SemiConductor and makes it more Suitable for electronic devices Such as diodes & transistors.

P-type :

When a small amount of trivalent impurity is added to a pure semiconductor it is called p-type.

trivalent impurities are also called acceptors. one acceptor impurity creates one hole in a p-type material and these holes are majority charge carriers.

Eg : Trivalent impurities are Gallium, Boron (or) Indium

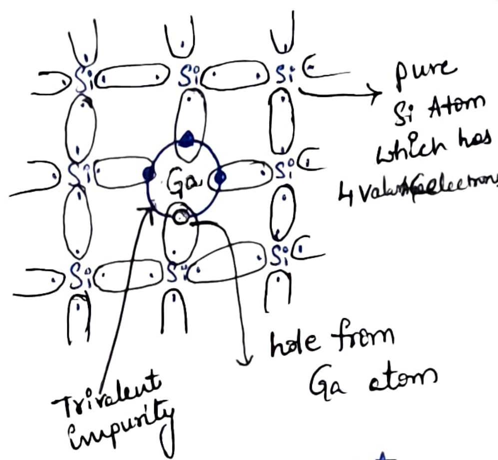


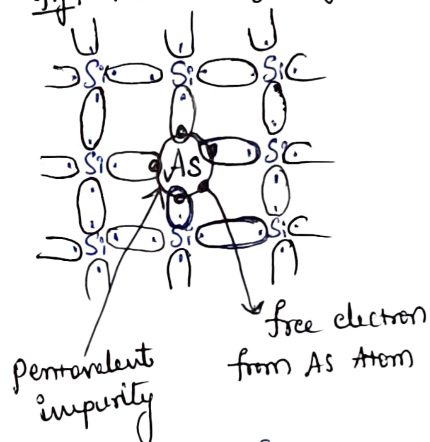
fig: Formation of p-type material.

N-type :

When a small amount of pentavalent impurity is added to a pure semiconductor it is called n-type.

pentavalent impurities such as arsenic, bismuth, phosphorous & antimony are called donor atoms. one donor impurity creates one free electron in n-type material and these free electrons are majority charge carriers.

fig: Formation of n-type material



1 b Forbidden Gap Energy levels :

Energy band :

The valance electrons posses highest energy level forms the covalent bonds, due to the coupling between the valence electrons the energy levels associated with the valance electrons merge into each other. This merging forms an energy band.

Similarly the energy levels of various electrons present in the first orbit, second orbit e.t.c also merge to form the various energy bands.

② a

The intrinsic Carrier Concentration(n_i) increases with temperature in both Ge and Si.
The intrinsic Carrier Concentration is the density of Charge Carriers in a pure SemiConductor material. It is higher in Ge than Si because Ge has a smaller energy band gap which makes it easier for electrons to be thermally excited from the valence band to the Conduction band.
Intrinsic Carrier Concentration for Ge is 2.5×10^{13} Cm^3 at 300°K while for Si is 1.5×10^{10} Cm^3
∴ It Can be Concluded at room temperature Ge has a higher intrinsic Carrier Concentration than Si atom.

② b

Effect of temperature on Conductivity in SemiConductors :

As temperature increases more number of electron-hole pairs are generated. Hence the Concentration of free electrons (n) & holes (p) also increases.
This leads to increase The value of intrinsic Concentration (n_i)
As n_i increases, σ_i is also increases while its resistivity decreases.
In pure Ge at room temperature, there exists one pair of electron & hole for every 2×10^9 Ge atoms.

$$n_i^2 = A_0 T^3 e^{-E_{G0}/KT}$$

→ This Equation shows the mathematical relation of intrinsic Carrier Concentration with temperature.

Where A_0 = Constant (independent of temperature

T = Absolute temperature in °K

E_{G0} = Forbidden energy gap at absolute Zero temperature

Valence Band:

The energy band formed due to merging of energy levels associated with the valence electrons.

Conduction Band:

It is formed due to merging of energy levels associated with the free electrons.

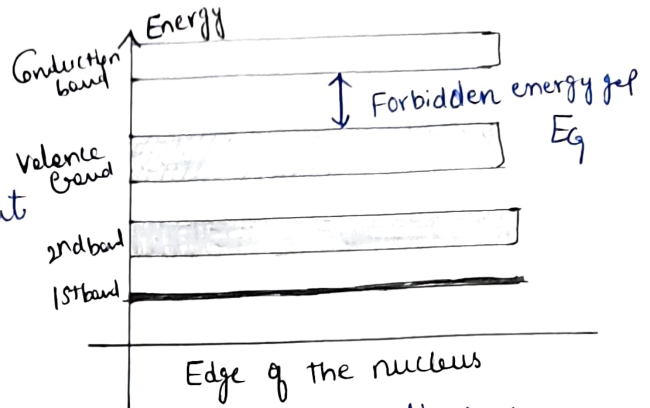


fig: Energy band diagram.

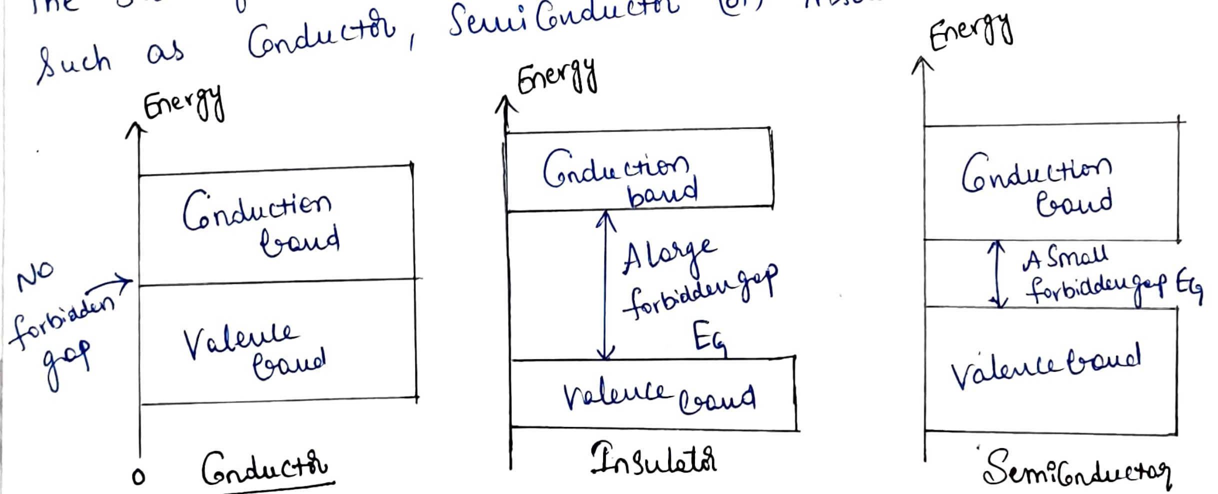
Forbidden Band (or) gap:

The energy gap which is present seperating the Conduction band & the valence.

Significance of forbidden gap:

The forbidden energy gap is the energy required to move electrons from the valence band to the Conduction band. Electrons in the valence band are tightly bound to the nucleus, so they can't move freely. They need to absorb enough energy to excite from valence band to Conduction band.

The size of the forbidden gap determines the type of material such as Conductor, Semi Conductor (or) insulator.

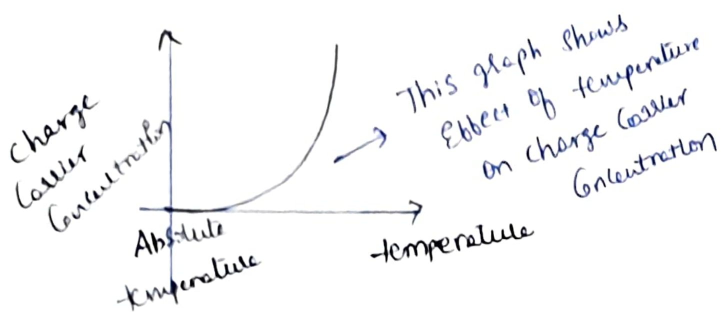


In Conductors forbiddengap Eg is 0ev.

In SemiConductors: Eg = 0.72ev for Ge

Eg = 1.12ev for Si

In insulators : Eg is about 7ev approximately



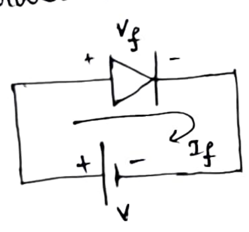
K = Boltzmann's Constant = 8.62×10^{-5} eV/°K

③ a

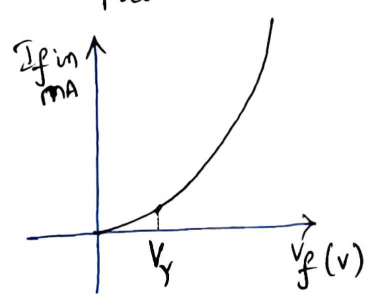
V-I Characteristics of PN Junction diode:

The response of p-n Junction Can be easily indicated with the help of characteristics called V-I characteristics of p-n junction diode. It is the graph of voltage applied across the p-n junction & the current flowing through the p-n junction.

Forward biased diode:



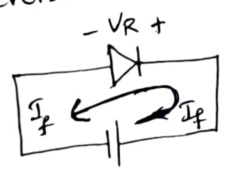
Forward characteristics of a diode



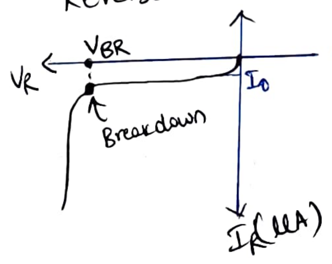
As long as $V_f < V_\gamma$ the current flowing is small. As V_f increases towards V_γ the width of depletion region goes on reducing.

When $V_f > V_\gamma$ the depletion region becomes very thin and current I_f increases suddenly. This incriment is exponential in nature.

Reverse biased diode:



Reverse characteristics of a diode

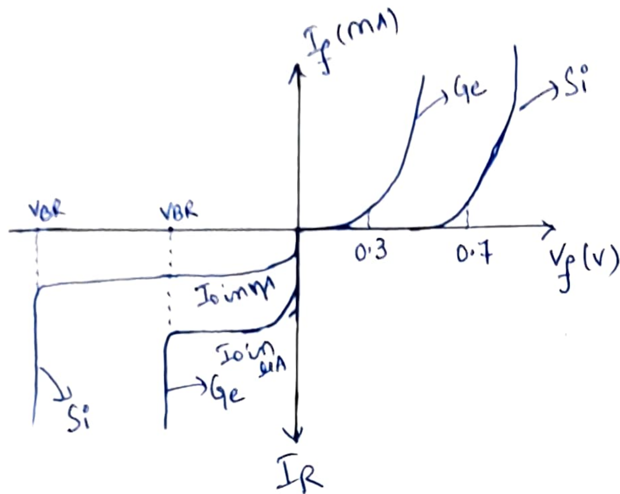


As reverse voltage increases Reverse Current increases initially but after certain voltage, the Current remains Constant equal to reverse Saturation Current I_o though reverse voltage is increased.

The voltage at which breakdown occurs is Called Reverse breakdown voltage (V_{BR}).

Reverse Current before the breakdown is very very small and Can be practically neglected.

V-I Characteristics of Si diode & Ge diode:



	V_γ	I_o	temperature
Si	0.7V	in nA	At higher temperature Not easily damaged
Ge	0.3V	in μA	destroyed at higher temperature

Breakdown voltage of Ge < Breakdown voltage of Si

③ b

Given data:

At 300°K $V_T = 26mv = 26\times10^{-3}V$

$V = 0.7V$ for $I = 2$ mA & $\eta = 2$ for Si

Solution: Diode Current Equation is given by

$$I = I_o\left(e^{V/\eta V_T} - 1\right)$$

$$2\times10^{-3} = I_o\left(e^{0.7/2\times26\times10^{-3}} - 1\right) \Rightarrow 2\times10^{-3} = I_o(701.89\times10^{3})$$

$$\therefore I_o = \frac{2\times10^{-3}}{701.89\times10^{3}} = 2.849 \text{ nA}$$

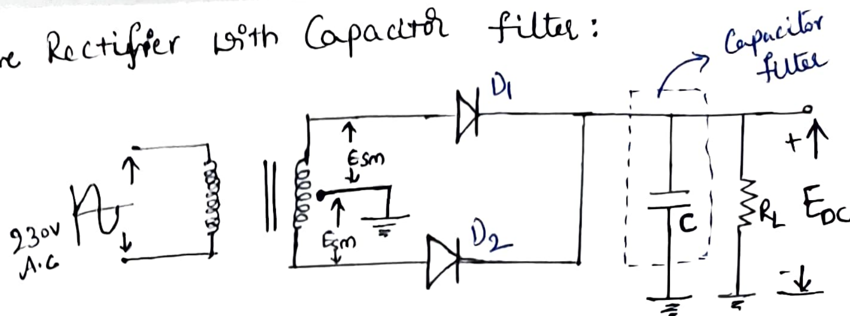
Now voltage increases to 0.75V ∴ V = 0.75V then

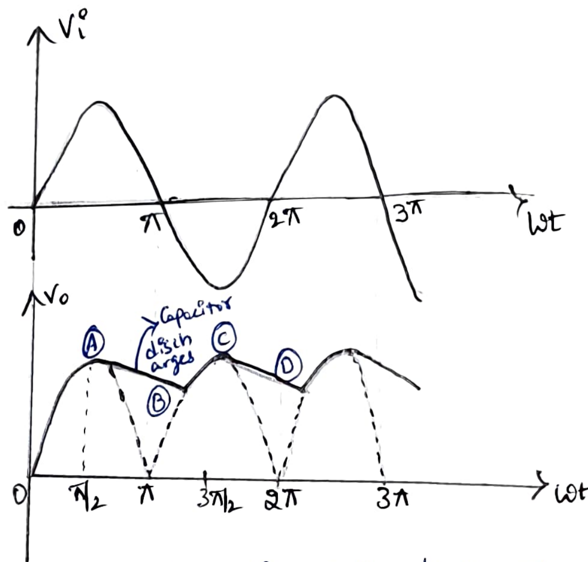
$$I = I_o\left(e^{0.75/2\times26\times10^{-3}} - 1\right)$$

$$I = 2.849\times10^{-9}\left(e^{0.75/2\times26\times10^{-3}} - 1\right)$$

$$I = 5.23\times10^{-3}A = 5.23 \text{ mA}$$

④ a **Circuit of fullwave Rectifier with Capacitor filter:**





Operation :

✓ When power is turned on, the Capacitor C gets charged through D_1 to E_{sm} during first quarter Cycle of the rectified output voltage.

✓ The next quarter cycle from 0 to π The Capacitor C starts discharging through R_L.

✓ once Capacitor gets charged to E_{sm} D_1 is reversebiased and turned off. So during $\pi/2$ to π Capacitor supplies load Current. It discharges to point B.

✓ At point B, lying in the quarter π to $\frac{3\pi}{2}$ of the rectified output voltage, the i/p voltage exceeds Capacitor voltage making D_2 forward biased. This charges Capacitor back to E_{sm} at point C.

✓ The time required by Capacitor C to charge to E_{sm} is small and only for this period D_2 is Conducting.

✓ Again at point C, D_2 stops Conducting & Capacitor supplies load and starts discharging upto point D in the next quarter Cycle of the rectified o/p voltage.

✓ At this point D_1 Conducts to charge Capacitor back to E_{sm}.

In this manner with the help of Capacitor filter, ripple factor value Can be decreased.

Thus the output Can be made smoother, reducing the ripple Content by selecting larger value of Capacitor.

4

4 b Ripple factor :

The amount of a.c content present in the output can be mathematically expressed by a factor called Ripple factor, indicated by γ. It tells how smooth is the output. Less is the ripple factor, better is the performance of the circuit.

$$\gamma = \frac{\text{Rms value of a.c Component of output}}{\text{Average (or) d.c Component of output}}$$

Peak Inverse voltage (PIV) :

It is the peak voltage across the diode in the reverse direction. i.e when the diode is reverse biased.

Diode must be selected based on the PIV Rating & the circuit specifications.

% Regulation :

As the load current changes, load voltage changes. practically load voltage should remain constant. The concept of regulation is to study the effect of change in load current on the load voltage.

$$\text{Voltage Regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

% Rectification :

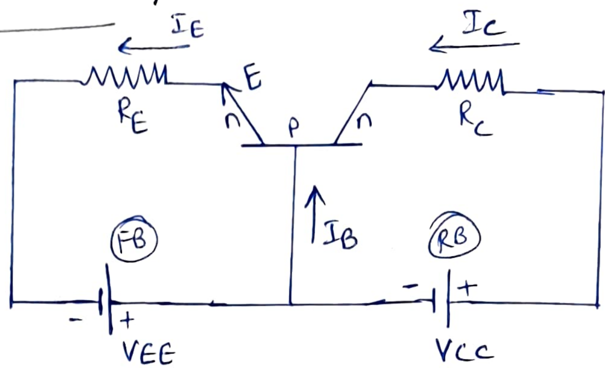
It signifies, how efficiently the rectifier circuit converts a.c power into d.c power.

$$\% \eta = \frac{P_{dc}}{P_{ac}}$$

Comparision :

Type of Rectifier / Parameter	Ripple factor(γ)	PIV	% η	% Regulation	Transformer utilization factor
Halfwave Rectifier	1.211	$E_{Sm} = \pi E_{DC}$	40.6%	$\frac{R_f}{R_L} \times 100$	0.287
Fullwave Rectifier	0.48	$2E_{Sm}$	81.2%	$\frac{R_f}{R_L} \times 100$	0.693

5 a Common Base Configuration :

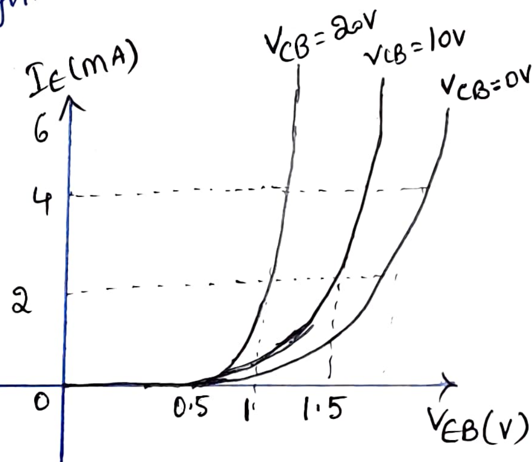


To understand Complete electrical behaviour of a transistor it is necessary to study the interrelation of the various Currents and voltages.

These relations Can be plotted graphically Known as Characteristics of transistor.

✓ In Common Base Configuration, the input impedance is Low and the output impedance is high.

Input Characteristics :



It is the Curve between i/p Current I_E and input voltage V_{EB} at Constant V_{CB}.

✓ V_{BE} is increased by Keeping V_{CB} Constant initially at zero and I_E is noted Similarly V_{CB} is increased and kept Constant. then V_{BE} is increased & the output Current I_E noted.

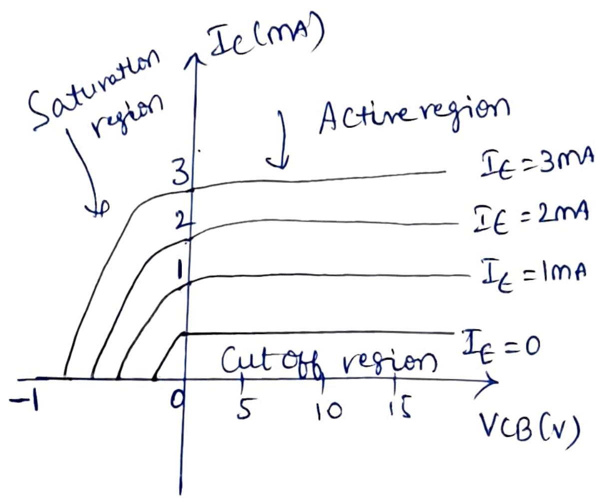
✓ Input side is forward biased so the input resistance is small so for a small increase in V_{BE} there is rapid increase in the emitter Current I_E.

✓ As the output voltage V_{CB} is increased the width of the depletion layer between emitter base decreases and the Cut in voltage reduced.

✓ So the Curve drifts to the left side.

Output characteristics:

It is the curve between Collector Current I_C & Collector base voltage V_{CB} at Constant Emitter Current I_E.



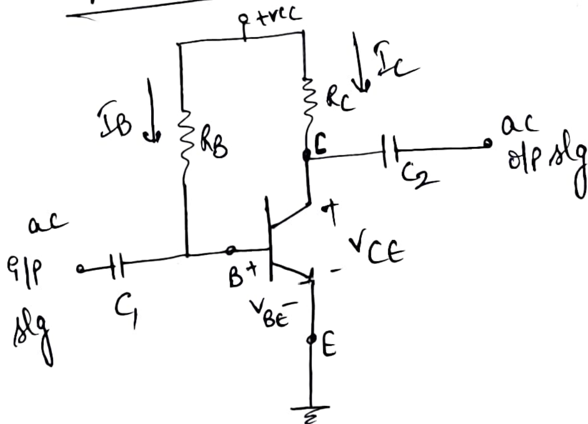
✓ When the input Current I_E is zero it is in Cutoff region and both the junctions are in reverse biased

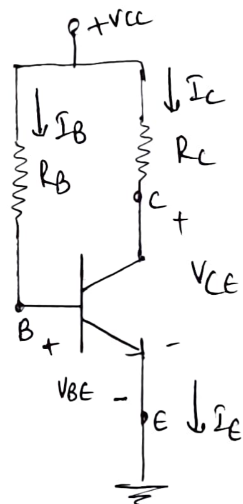
✓ In saturation region both emitter base junction & Collector base junction are forward biased. It is the region which is to left of $V_{CB} = 0V$

✓ In active region I_E is gradually increases and kept Constant output voltage V_{CB} is increased further and the output Current I_C almost remains Constant. Hence in active region curve is almost flat. Output voltages causes only a very little change in output Current.

5 b

Fixed Bias Circuit:





D.C Equivalent Circuit

It is one of the Stabilization techniques which allow I_B to vary so as to keep I_C relatively Constant with variation in I_{CO}, β & V_{BE}.

It is the simplest d.c bias Configuration.

DC Analysis :

For base circuit : Apply KVL

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow I_C = \beta I_B$$

For Collector Circuit : Apply KVL

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore \boxed{V_{CE} = V_{CC} - I_C R_C}$$

From I_B Equation it is observed base current is Controlled by R_B & I_C is related to I_B. I_C is independent of R_C. changing R_C value to any level will not affect the level of I_B (or) I_C as long as we remain in the active region of the device.

Stability factor of fixed bias Circuit :

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

W.K.T $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ but V_{CC} & V_{BE} are Constants and it doesn't Contain I_C term

Hence $\frac{\partial I_B}{\partial I_C} = 0$

$$\therefore S = \frac{1+\beta}{1-0} = 1+\beta \Rightarrow \boxed{S = 1+\beta}$$

(6) a

Current amplification factors

It is also known as Current gain and is the ratio of output Current to input Current. It is a measure of how much an analog amplifier boosts the strength of a signal.

The Current amplification factor depends on the mode of transistor

Current amplification factor of CE Configuration (β_{dc}):

$$\beta_{dc} = \frac{I_C}{I_B}$$

$\alpha_{dc} = \frac{I_C}{I_E}$ is for CB Configuration and $\gamma_{dc} = \frac{I_E}{I_B}$ for CC Configuration

there is a relation between α, β & γ

W.K.T $I_E = I_C + I_B$

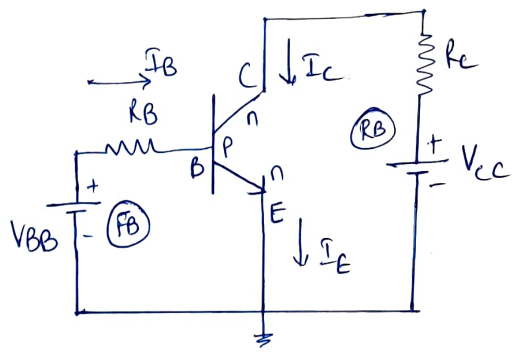
Divide both sides by I_B

$$\therefore \frac{I_E}{I_B} = \frac{I_C}{I_B} + \frac{I_B}{I_B} \Rightarrow \boxed{\gamma = \beta + 1}$$

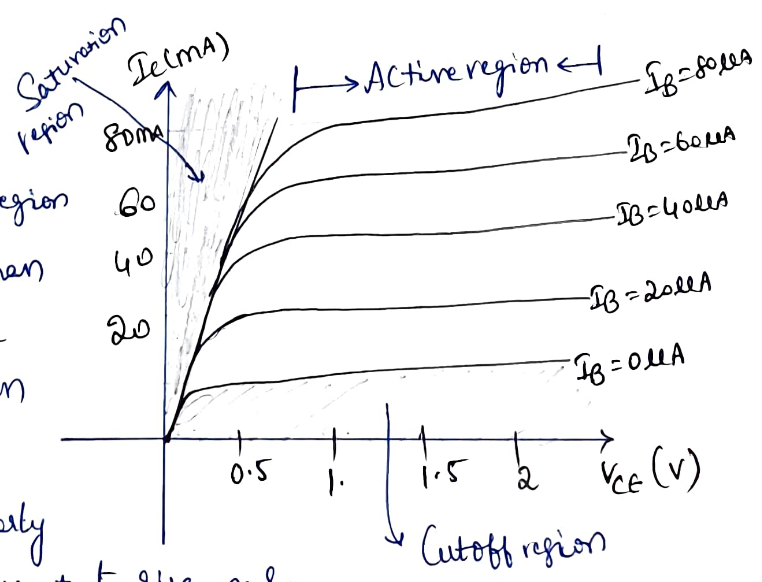
$$\text{W.K.T } \beta = \frac{\alpha}{1-\alpha} \Rightarrow \therefore \gamma = \frac{\alpha}{1-\alpha} + 1 \Rightarrow \boxed{\gamma = 1 + \beta = \frac{1}{1-\alpha}}$$

(6) b **Common Emitter Circuit of a junction transistor**

In this Configuration Emitter terminal is made Common for Base & Collector terminal.



Output Characteristics :



Active region:

As V_{CE} increased, reverse bias increases. This cause depletion region to spread more in base than in Collector, reducing the chances of recombinations in the base. This increases the value of α_{dc}. This early effect causes Collector Current to rise more sharply with increasing V_{CE} in the linear region.

In this region I/P Junction(J_E) is Forward biased and O/P Junction(J_C) is Reverse biased.

Saturation region :

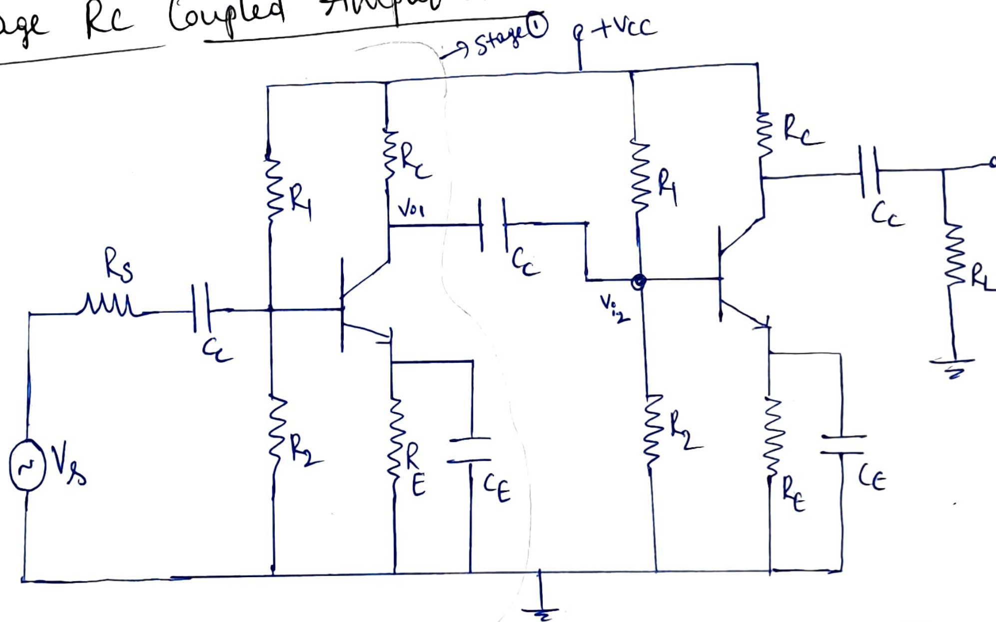
When both the junctions are Forward biased the transistor operates in this region usually V_{CE} sat ranges between 0.1V to 0.3V.

Cutoff region :

When the input base Current is =0, the Collector Current is the reverse leakage Current I_{CEO}. The region below $I_B=0$ is the Cutoff region. In this region both the junctions are in reverse biased mode.

⑦ a

Two Stage RC Coupled Amplifier :



✓ Output of Stage ① is Coupled as input to the Stage ② with the help of Coupling Capacitor.

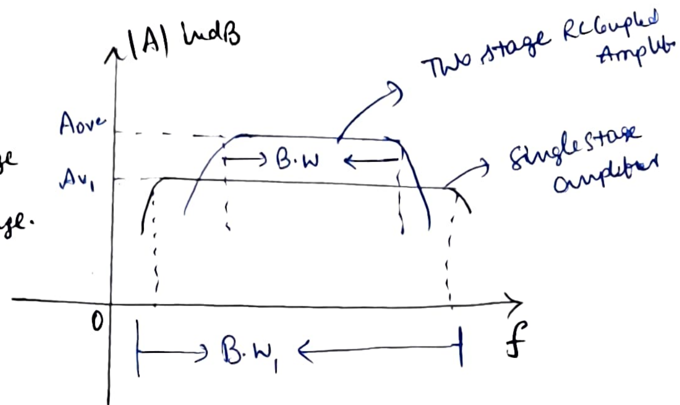
✓ Stage ① produces 180° phaseshift at its output. It is feed to the Stage ② amplifier. Hence O/P of two stage amplifier is having 0° phase shift and amplified further.

$$A_{overall} = A_{v1} \times A_{v2} = \frac{V_{o2}}{V_s} = \frac{V_{o2}}{V_{o1}} \times \frac{V_{o1}}{V_s}$$

$$\boxed{A_v = A_{v1} \times A_{v2}}$$

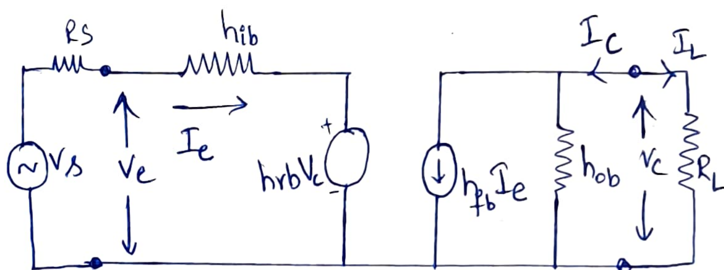
Frequency Response :

B.W of Two stage < B.W of 1st stage
Gain of Two stage > Gain of 1st stage.



(7) b) Transistorized amplification parameters of CB Configuration

h-parameter model of CB amplifier:



To find Current gain A_i :

$$A_i = \frac{I_L}{I_e} = \frac{-I_c}{I_e}$$

$$I_c = h_{fb} I_e + h_{ob} V_c = h_{fb} I_b + h_{ob}(-I_c R_L)$$

$$I_c (1 + h_{ob} R_L) = h_{fb} I_e$$

$$\boxed{A_i = \frac{-I_c}{I_e} = \frac{-h_{fb}}{1 + h_{ob} R_L}}$$

Input Resistance R_i :

$$R_i = \frac{V_e}{I_e}$$

$$V_e = h_{ib} I_e + h_{rb} V_c = h_{ib} I_e + h_{rb}(-I_c R_L)$$

Divide by I_e on both sides

$$\frac{V_e}{I_e} = h_{ib} + h_{rb}\left(\frac{-I_c}{I_e}\right) R_L$$

$$\boxed{R_i = \frac{V_e}{I_e} = h_{ib} + h_{rb} A_i R_L}$$

Voltage gain: $A_v = \frac{V_c}{V_e} = \frac{A_i I_e R_L}{V_e} = \frac{A_i R_L}{R_i} \Rightarrow$ $\boxed{A_v = \frac{A_i R_L}{R_i}}$

Output admittance Y_0: $Y_0 = \frac{I_c}{V_c}\Big|_{V_S=0}$

$$I_c = h_{fb} I_e + h_{ob} V_c$$

$$\frac{I_c}{V_c} = \frac{h_{fb} I_e}{V_c} + h_{ob}$$

KVL at i/p loop with $V_S = 0$ then

$$R_S I_e + h_{ib} I_e + h_{rb} V_c = 0$$

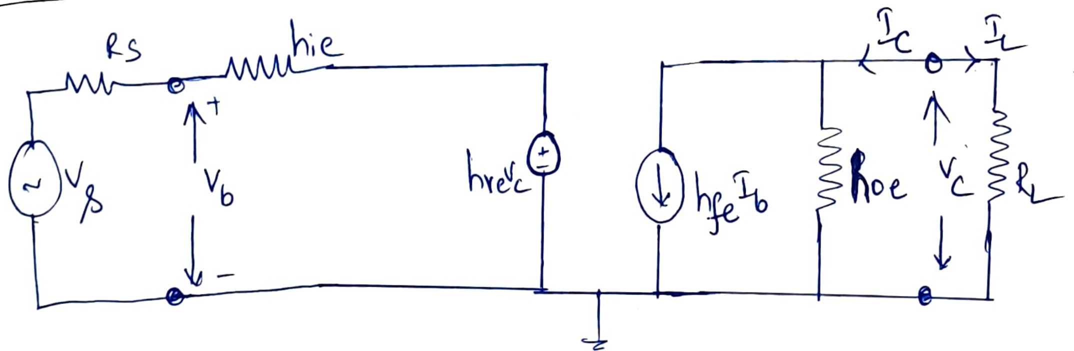
$$(R_S + h_{ib}) I_e = -h_{rb} V_c$$

$$\frac{I_e}{V_c} = \frac{-h_{rb}}{R_S + h_{ib}}$$

$$Y_0 = \frac{I_c}{V_c} = h_{fb}\left(\frac{-h_{rb}}{R_S + h_{ib}}\right) + h_{ob}$$

$$\boxed{Y_0 = h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}}$$

8 a Transistorized amplification parameters for CE Configuration



Current gain A_i:

$$A_i = \frac{I_L}{I_b} = \frac{-I_c}{I_b}$$

$$I_c = h_{fe} I_b + h_{oe} V_c = h_{fe} I_b + h_{oe}(-I_c R_L)$$

$$(1 + h_{oe}) I_c = h_{fe} I_b$$

$$\frac{I_c}{I_b} = \frac{h_{fe}}{1+h_{oe}R_L} \Rightarrow \boxed{A_i = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1+h_{oe}R_L}}$$

Input Resistance R_i :

$$R_i = \frac{V_b}{I_b} \quad \text{but} \quad V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re}\frac{V_c}{I_b} = h_{ie} + h_{re}\left(-\frac{I_c}{I_b}\right)R_L$$

$$\boxed{R_i = h_{ie} + h_{re} A_i R_L}$$

Voltage Gain A_v :

$$A_v = \frac{V_c}{V_b} = \frac{A_i I_b R_L}{V_b} = \frac{A_i R_L}{R_i} \Rightarrow \boxed{A_v = \frac{A_i R_L}{R_i}}$$

Output Admittance Y_o :

$$Y_o = \left.\frac{I_c}{V_c}\right|_{V_s=0}$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = \frac{h_{fe} I_b}{V_c} + h_{oe}$$

KVL at input loop with $V_s = 0$

$$R_s I_b + h_{ie} I_b + h_{re} V_c = 0$$

$$(R_s + h_{ie}) I_b = -h_{re} V_c \Rightarrow \frac{I_b}{V_c} = \frac{-h_{re}}{R_s + h_{ie}}$$

$$\therefore \quad Y_o = h_{oe} + h_{fe}\left(\frac{-h_{re}}{R_s + h_{ie}}\right)$$

$$\boxed{Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}}$$

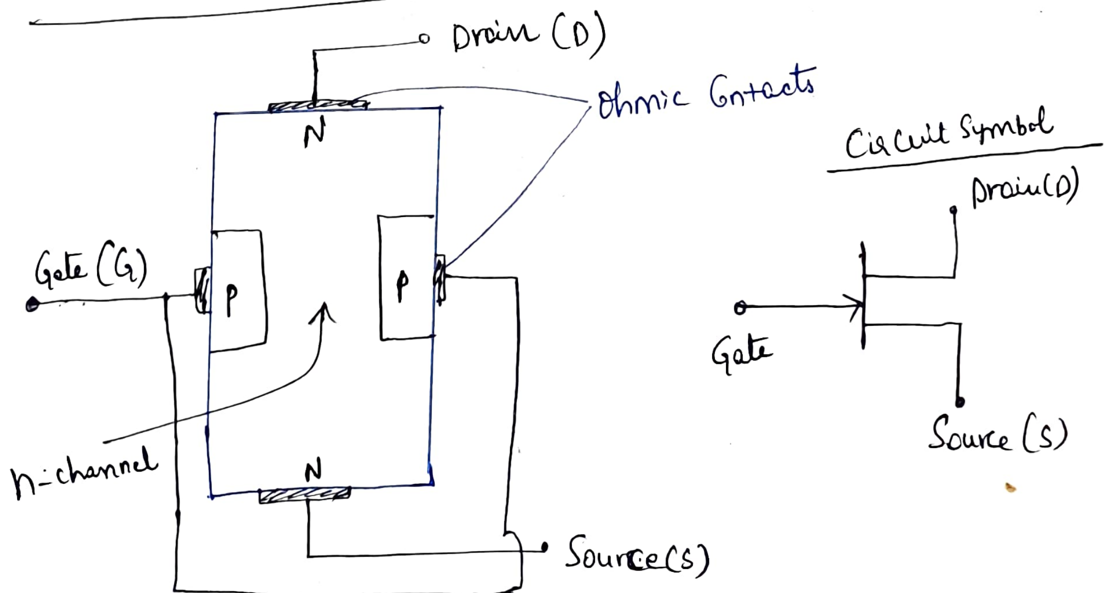
8 b

Comparision of transistorized Amplification parameters

parameter / Configuration	Common base	Common Emitter	Common Collector
Current gain (A_i)	< 1 $A_i = \frac{-h_{fb}}{1+h_{ob}R_L}$	High $A_i = \frac{-h_{fe}}{1+h_{oe}R_L}$	High $A_i = \frac{-h_{fc}}{1+h_{oc}R_L}$
Voltage gain (A_v)	medium $A_v = \frac{A_i R_L}{R_i}$	medium $A_v = \frac{A_i R_L}{R_i}$	< 1 $A_v = \frac{A_i R_L}{R_i}$
I/p resistance (R_i)	very Low (2Ω) $R_i = h_{ib} + h_{rb} A_i R_L$	Low ($1k\Omega$) $R_i = h_{ie} + h_{re} R_i A_L$	High ($500 k\Omega$) $R_i = h_{ic} + h_{rc} R_i A_L$
O/p resistance (R_o)	Very high ($1M\Omega$)	High ($40k\Omega$)	Low (50Ω)
O/p admittance (Y_o)	$h_{ob} - \frac{h_{rb} h_{fb}}{R_s + h_{ib}}$	$h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}$	$h_{oc} - \frac{h_{rc} h_{fc}}{R_s + h_{ic}}$

9 a

Construction of JFET : (n-channel)



Operation :

Case i : When V_{GS} & V_{DS} both = 0

Drain Current doesn't flow $\therefore I_D = 0$

Case ii : When $V_{GS} = 0$ and vary V_{DS} i.e $V_{GS} \geq 0$

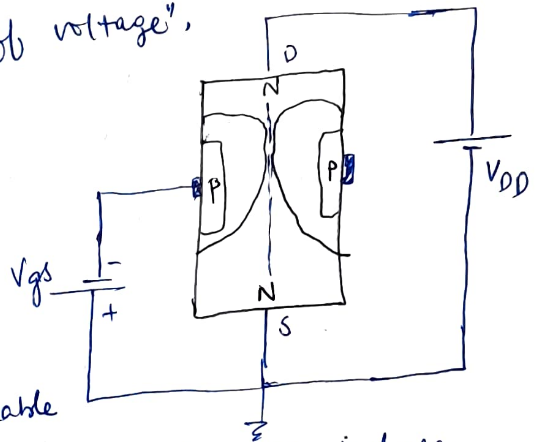
V_{DS} increases further maximum drain current I_{DSS} flows

when V_{GS} = Constant and vary V_{DS}

V_{DS} increases further drain Current I_D increases.

At Some value of V_{DS} drain Current I_D Cannot be increased further due to reduction in channel width.

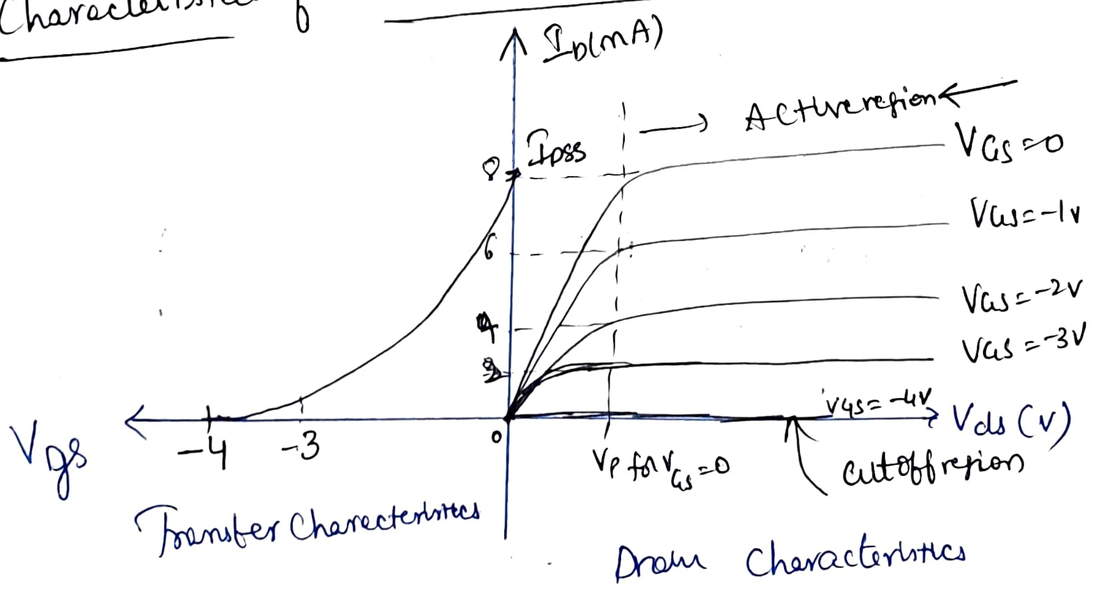
The Voltage V_{DS} at which the Current I_D reaches to its Saturation level is Called "pinch off voltage".



Case iii : When $V_{gs} < 0$

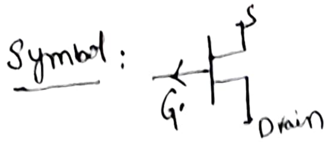
When $V_{gs} = -1V$ is applied between gate & Source, the gate channel junctions are further reverse bias reducing the Effective width of channel available for the Conduction. Because of this drain current will reduce and pinchoff Voltage is reached at lower drain current.

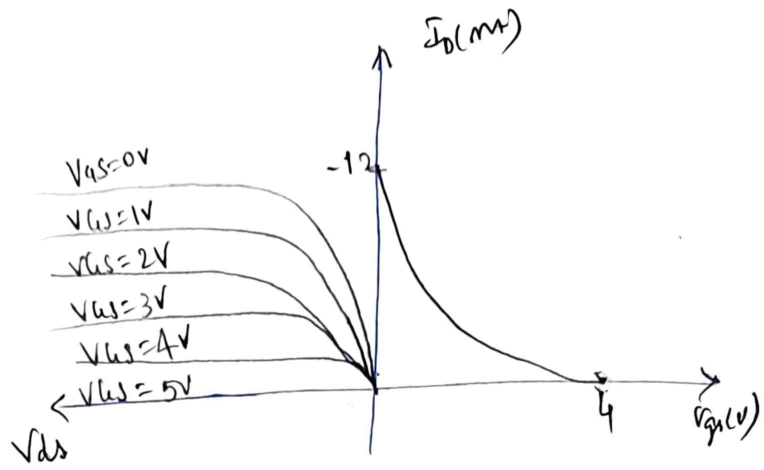
Characteristics of n-channel JFET



P-channel JFET : Substrate is n-type & Channel is ptype bar

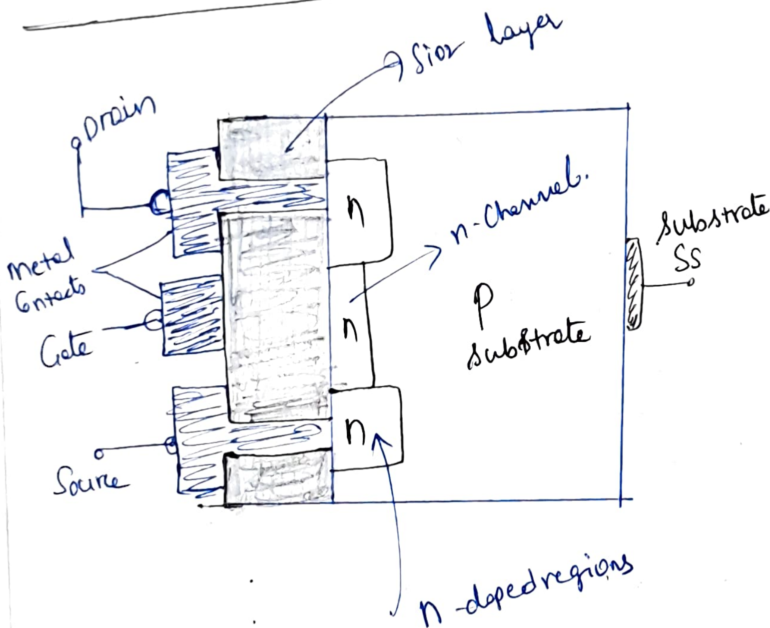
Symbol :



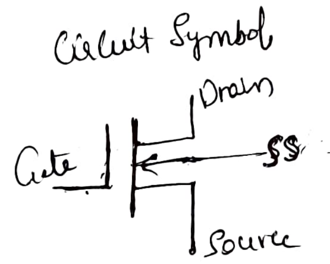


9 b

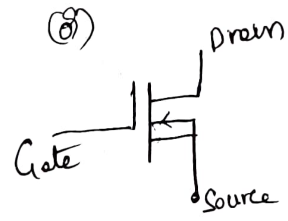
N-Channel MOSFET :



Circuit Symbol

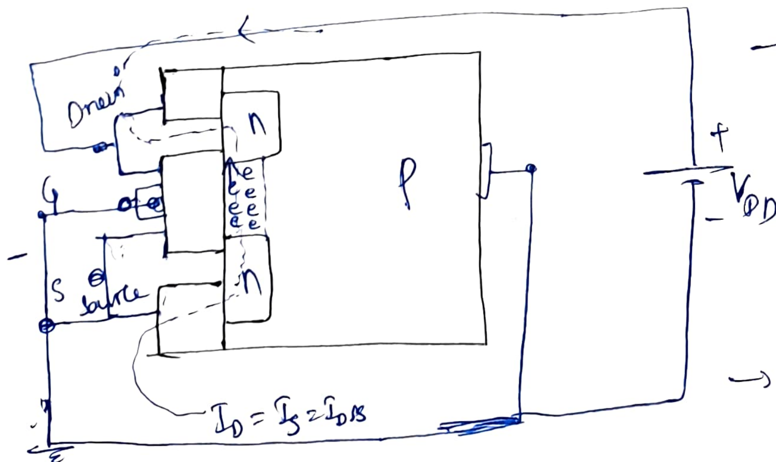


(or)



Case i : When V_{GS} & V_{DS} = 0 No drain Current flows i.e. $I_D = 0$

Case ii : When $V_{gs} \geq 0$ & V_{GS} = Constant



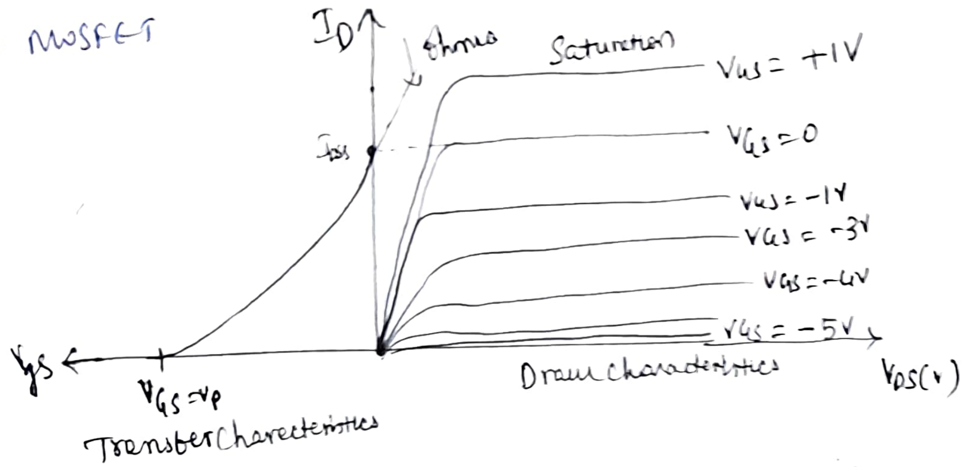
→ When V_{gs} is negative electrons repelled by negative potential I_D decreases.

→ When V_{gs} is positive I_D increases

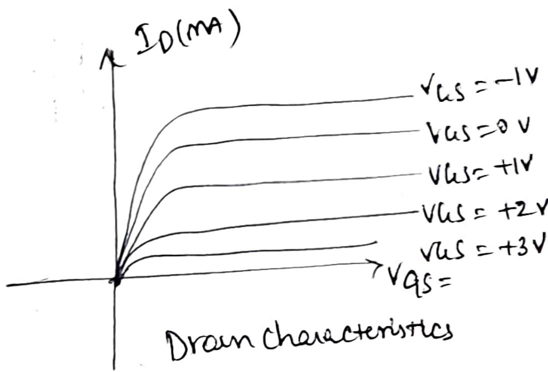
✓ $I_D = 0$ Corresponds to $V_{GS}(off)$, $V_{GS}(off) = -V_P$

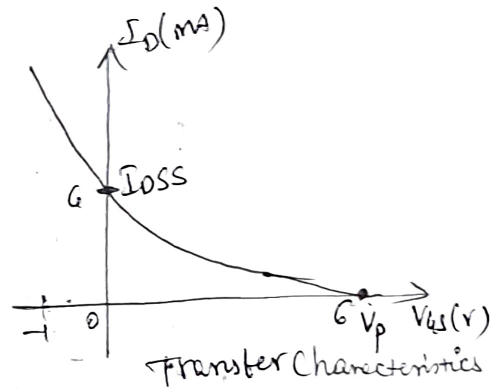
✓ $V_{GS} = 0$ Corresponds to I_{DSS}

✓ Both positive & Negative values of V_{GS} can be used to bias depletion MOSFET

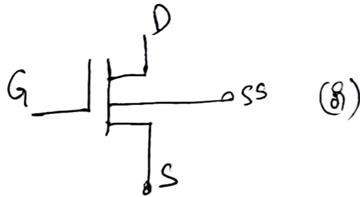


For P-channel Depletion MOSFET





Circuit Symbol



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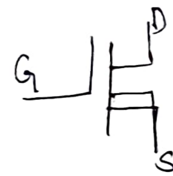

(10) a

Transconductance :

indicated by g_m.

It is one of the important parameters of JFET.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Bigg|_{V_{DS} = \text{Constant}}$$

It can be measured from the transfer characteristics.

Amplification parameter : (a) Amplification factor (μ) :

In JFET, Drain to source current of is controlled by gate to source voltage. The relation between output & input quantity is given by transconductance factor(g_m).

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Bigg|_{I_D = \text{Constant}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{gs}} = r_d \, g_m$$

$$\therefore \boxed{\mu = g_m r_d}$$

Pinchoff voltage (V_P) :

The pinchoff voltage in a MOSFET is the voltage at which the channel of the MOSFET closes.

It is the gate-source voltage level at which MOSFET enters saturation and the channel becomes effectively "pinched off".

$$V_{ds} = V_p = V_{gs} - V_T$$

V_{ds} → Drain to Source voltage

V_{gs} → Gate to Source voltage

V_T → Threshold voltage.

10 b Comparision of FET and BJT

S.No	Parameter	FET	BJT
1.	Control element type	Voltage Controlled device	Current Controlled device
2.	Type of device	Unipolar	Bipolar
3.	Current Conduction	due to majority Carriers	due to both majority & minority Charge Carriers
4.	terminals	Source, Gate & Drain	Emitter, Base & Collector
5.	Configurations	CS, CG & CD	CE, CB & CC
6.	Size	Small	Big
7.	Thermal Stability	is more	is Less
8.	Sensitivity	Less Sensitivity to changes in applied voltage	Higher Sensitivity to changes in the applied signals.
9.	Thermal Runaway	Doesnot Exist	Exists
10.	Input Resistance	High	Low
11.	Thermal Noise	Low	More
12.	Ratio of output to input (Amplification factor)	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$	$\beta = \frac{\Delta I_C}{\Delta I_B}$

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